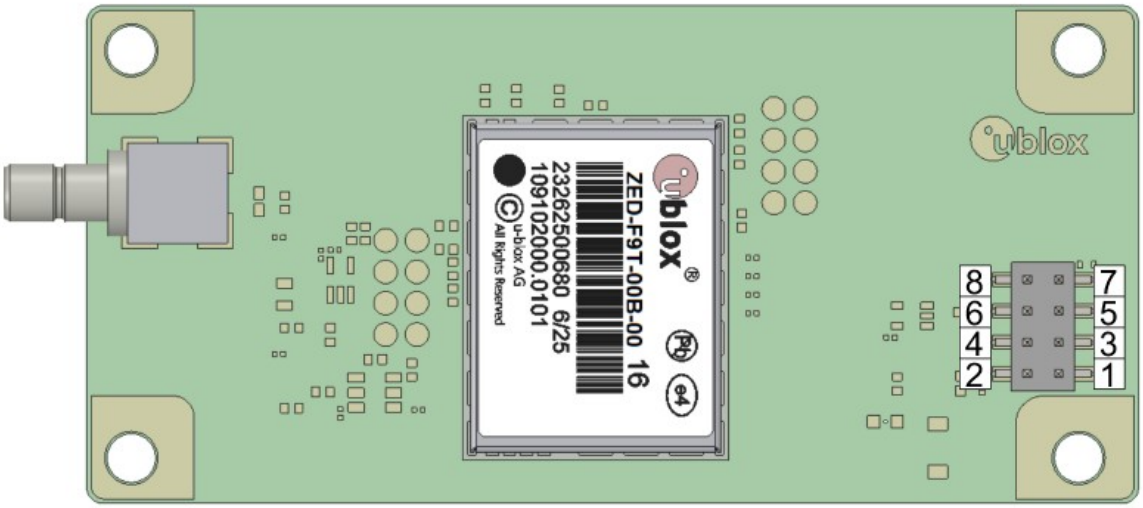
Connection of Ublox RCB-F9T to the RAD-CELF board



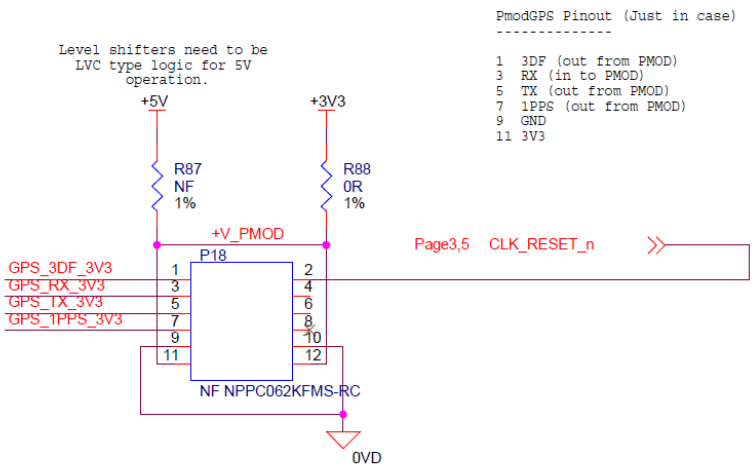
UBLOX GPS Module Connector

Pin No	Name	I/O	Description
1	VCC_ANT	I	Antenna power supply. 5.0 V max 100 mA
2	VCC	I	Operating voltage, 3.3 V
3	TXD	O	UART TXD, LVCMOS, From Module
4	RST	I	Hardware reset
5	RXD	I	UART RXD, LVCMOS, To Module
6	TP1	O	Time Pulse 1, LVCMOS
7	TP2	O	Time Pulse 2, LVCMOS
8	GND	-	0V Ground

RAD-CELF PMOD Connector

Pin No	Name	I/O	Description
1	GPS_3DF	I	GPS 3D Fix, LVCMOS
2	RESET_n	O	System Reset,, LVCMOS
3	RXD	O	UART RXD, LVCMOS, From ACQ1001
5	TXD	I	UART TXD, LVCMOS, To ACQ1001
7	GPS_1PPS	I	PPS Time Pulse , LVCMOS
9,10	0VD	-	0V Ground
11,12	VCC	O	3.3V VCC
4,6,8	NC	-	No Connect

This is shown in the schematic fragment below



UBLOX to RAD-CELF Connections

Basic UART is straight forwards, definitions are the same so no need to cross the wires between the RCB-F9T and the RAD-CELF simply connect RXD on the RAD-CELF to RXD on the RCB-F9T and the same for the TXD

Timing Signals – the RCB-F9T has 2 but the RAD-CELF only one but there is no 3DF on the RCB-F9T so simply connect the two timing signals in both boards

3.3V and 0V again simple

Reset on the RAD-CELF is active low and on the RCB-F9T it is active high so cannot be used – After further testing it was decided to not use the Reset signal as a soft reset was available using a serial port command.

There is no +5V on the PMOD for the RCB-F9T antenna however there is a header P17 close to the PMOD that can be used. This is only for local testing – an external supply will be used by the end user.

Cable Specification

The housing for the 2mm connector on the RCB-F9T selected is Farnell 3049214 with crimps Farnell 2293846 with say 6” of wire to the RAD CELF

The wire up of the cable between the RCB-F9T and the RAD CELF is therefore

Pin No	Name	Description	Connection on RAD-CELF
1	VCC_ANT	Antenna power supply. 5.0 V max 100 mA	P17 Site Pin 1 – or Left for external connection
2	VCC	Operating voltage, 3.3 V	P18 Site Pin 11 or 12
3	TXD	UART TXD, LVCMOS, From Module	P18 Site Pin 5
4	RST	Hardware reset	Not Used
5	RXD	UART RXD, LVCMOS, To Module	P18 Site Pin 3
6	TP1	Time Pulse 1, LVCMOS	P18 Site Pin 7
7	TP2	Time Pulse 2, LVCMOS	P18 Site Pin 1
8	GND	0V Ground	P18 Site Pin 9 or 10

FPGA changes

Summary of UART connections

Name	UBLOX (DTE)	RAD CELF	Zynq UART (DTE)
RXD	Input	From ACQ1001 to GPS	Input
TXD	Output	To ACQ1001 from GPS	Output

Since both the UBLOX and the Zynq are DTE the FPGA shall do the TXD → RXD twist, this shall be done at the top level of the RAD-CELF logic.

Functional changes

FPGA change to put up the 25MHz (100 MHz / 4) clock counter derived from the secondary clock switch port 4. This will be set to the remapping DDS-C, counter is latched every PPS

The GPS PPS shall trigger the chirp on a given second. Software to tee up the trigger in the preceding second so that the PPS edge triggers the DDS system accurately.
Need additional FPGA register bit(s) to allow setting for GPS PPS driven IO Update and switching off External and existing Internal modes.
Need to check if TP1 or TP2 from GPS to be used as PPS signal code up for both - add both to TRIG or SYNC bus ?
Need to map GPS to a bit on the TRIG bus to sync ACQ43X, what clock source does the ACQ435 use ? - currently CLK_B_GEN i.e Oscillator at present