Hardware Installation Guide

ACQ1001, ACQ1002

Single/Dual-Site D-TACQ ELF/FMC Carrier

1 Overview

ACQ1001 is a miniature carrier designed to accommodate a single D-TACQ ELF[1] or FMC[2] module, allowing up to 32 simultaneous analogue data acquisition channels in one enclosure.

ACQ1002 is designed to accommodate up to two D-TACQ ELF modules, or an D-TACQ ELF module and an FMC module, allowing up to 64 simultaneous analogue data acquisition channels in one enclosure.

Both systems use a Xilinx Zynq-7000 All Programmable SoC Z-7020 running Linux. Connectivity is provided by gigabit Ethernet. External Clock and Trigger inputs are also provided, and multiple units may be synchronised together.

Expansion options are provided on ACQ1002 and include internal and external USB 2.0 connections and an external SD Card allowing for storage expansion, and PMOD connectivity for custom user modules such as GPS sync inputs respectively.

ACQ1001 and ACQ1002 are designed to fit up to 5 units within a 1U, 19” rack. ACQ1002 also ships in a compact configuration for use in PIGs or other space-restricted applications. Please see section 6 for rack-mount options and section 7 for dimensions.

2 Variations

ACQ1001 and ACQ1002 come in several standard configurations.

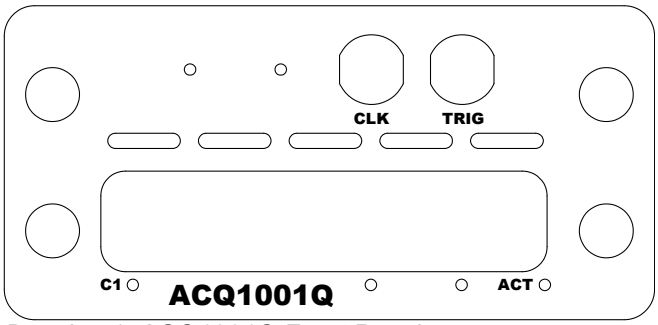
Product Name	***Compatibility***		
	D-TACQ or Third-Party FMC	**D-TACQ ELF**	***Form Factor***
ACQ1001Q-ELF		1x	Single
ACQ1001Q-FMC	1x		Single
ACQ1002R-ELF		2x	Rack
ACQ1002R-FMC	1x	1x	Rack
ACQ1002S-ELF		2x	Stack
ACQ1002S-FMC	1x	1x	Stack

Analogue voltage is set to ±15V as standard, but please contact D-TACQ for alternatives.

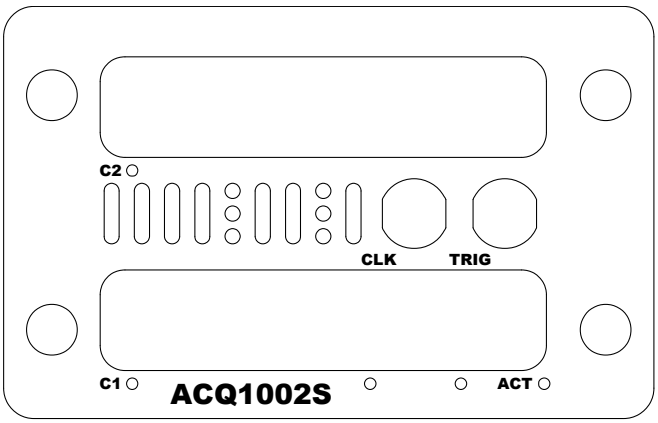
Third-party FMC modules may not be compatible with the D-TACQ mechanical superset of the FMC specification and undesired effects may occur. ACQ1001Q-ELF and ACQ1002R/S-ELF include power rails on the mezzanine connectors for D-TACQ ELF cards and therefore only use certain pins for FPGA connections. If third-party FMC modules need to be used with a D-TACQ ELF carrier, please contact D-TACQ for details on compatibility.

1 ELF – D-TACQ Mechanical Superset of FMC Standard
2 FMC – FPGA Mezzanine Card, ANSI/VITA 57.1

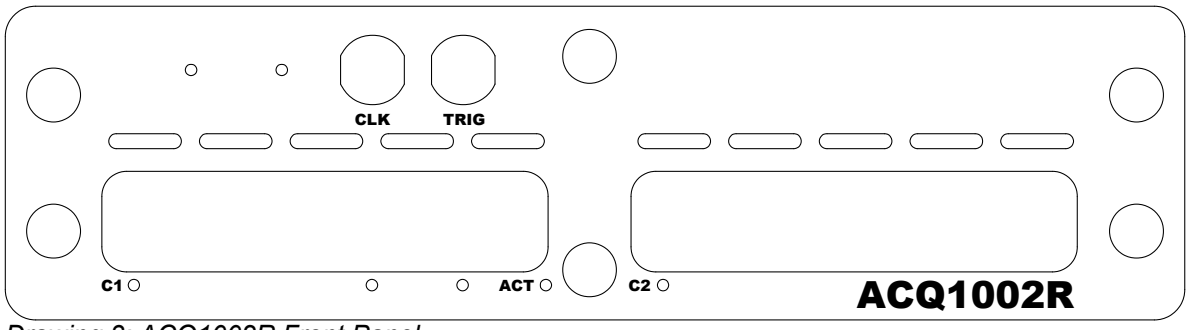
3 Front Panels



Drawing 1: ACQ1001Q Front Panel



Drawing 2: ACQ1002S Front Panel



Drawing 3: ACQ1002R Front Panel

3.1 D-TACQ ELF/FMC Sites

ACQ1001 and ACQ1002 have space for one or two D-TACQ ELF or FMC modules as described above. Please contact D-TACQ for details on our range of modular data acquisition cards, and see section 5 for details on field replacement.

3.2 LEDs

Upon power-up, the POWER LED (on the rear panel) should light, followed 20s later by LOADED (also on the rear panel) to indicate loading of the FPGA. When Linux boots, an LED test sequence will be shown, showing red and green on each LED.

LED	***Description***	
C1,C2	Red	Card present, invalid configuration. Analogue Power disabled if any card is invalid.
	Green	Card present, valid configuration. Analogue power enabled if all cards are valid.
CLK	Red	Unused at present.
	Green	Lit when a valid clock signal is in use.
TRIG	Red	Unused at present.
	Green	Lit when a valid trigger signal is being received on the front panel connector.
ACT	Green	Heartbeat – flashes to indicate Linux activity.

3.3 Clock

ACQ1001 and ACQ1002 accept a clock signal via a centre-positive single-pin LEMO 00 Series Mini Coax connector (part ERA.00.250.NTL). Mating plugs should be compatible with this part.

It is common practice for customers to manufacture their own cables to fit in with their own requirements.

3.4 Trigger

ACQ1001 and ACQ1002 accept a trigger signal via a centre-positive single-pin LEMO 00 Series Mini Coax connector (part ERA.00.250.NTL). Mating plugs should be compatible with this part.

It is common practice for customers to manufacture their own cables to fit in with their own requirements.

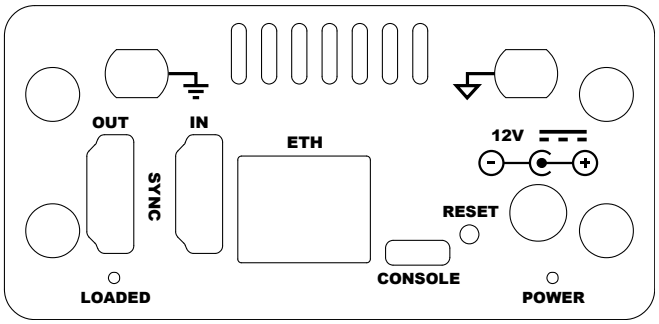
3.5 Optional LEMO connections

ACQ1001 and ACQ1002 can be fitted with up to two extra front panel LEMO connectors on request. These are bidirectional and may be used for both inputs or outputs. Please contact D-TACQ for more details.

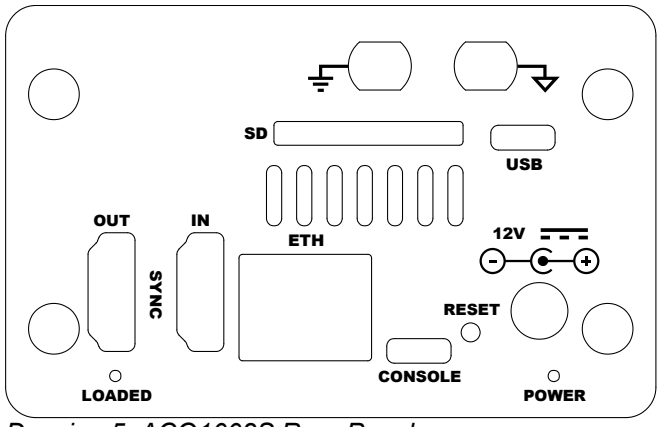
3.6 Air Inlets

The row of slots on the front panel allow air to enter ACQ1001 and ACQ1002, drawn across the cards by the rear fans. Do not cover the air inlets.

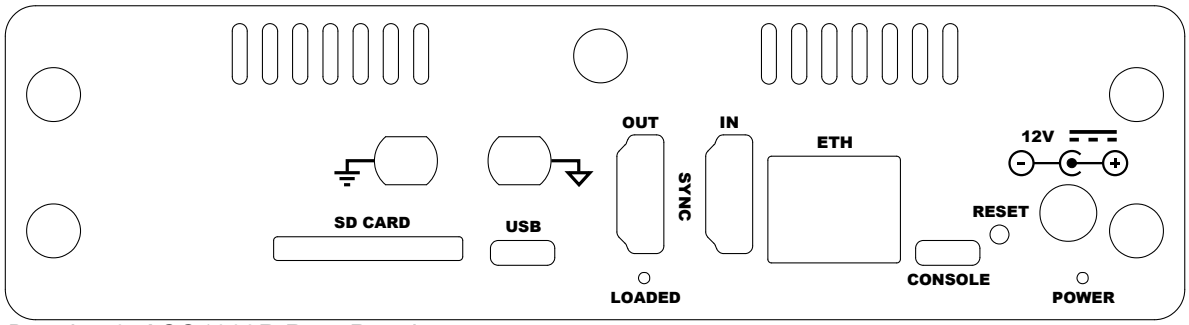
4 Rear Panels



Drawing 4: ACQ1001Q Rear Panel



Drawing 5: ACQ1002S Rear Panel



Drawing 6: ACQ1002R Rear Panel

4.1 Both ACQ1001 and ACQ1002

4.1.1 Console

ACQ1001 uses an FTDI FT232 USB-Serial converter for console access via a Micro USB port. Please see the FTDI website for drivers. Serial Console settings are as follows.

Name	***Setting***
Baud Rate	115200
Data Bits	8
Parity	No
Stop Bits	1
Flow Control	None

Note that on ACQ1001 the console connector may be reconfigured to provide a USB 2.0 OTG port instead of a console. Please contact D-TACQ if this is desired.

4.1.2 Ethernet

The gigabit Ethernet port accepts standard RJ45 connectors.

4.1.3 Reset

Use a pen or similar object to push the reset button if required.

4.1.4 Power

Power is provided to ACQ1001 and ACQ1002 by an external 12V regulated DC supply, of minimum output 10W depending on payload. The unit ships with a 45W 12V DC supply, sufficient for any payload combination.

The socket accepts a standard DC barrel connector, centre-positive, 2.5mm internal diameter, 5.5mm external diameter, with length a minimum of 10.5mm.

The power supply's input Earth should be connected to the output 0VD.

4.1.5 LEDs

The rear panel provides extra LEDs for system information.

LED	***Description***	
LOADED	Green	Lights approximately 20s after power-up to indicate FPGA loaded. If unlit after this, check the validity of the SD card image or check the Console for error messages.
POWER	Green	Lit when digital power supplies are all valid.

4.1.6 Sync Bus

D-TACQ provides two Sync Bus connectors allowing multiple units to be chained together. The bus uses standard HDMI cables and has two ports – one input, one output. The pinouts and functionality are described as follows.

Devices are able to communicate over I^2C if required.

Pin	***Name***	***Description***	
		Output	***Input***
1	Sync	Synchronisation Output	Synchronisation Input
4	Trigger	Trigger Output	Trigger Input
7	GPIO	General Purpose Output. May be switched to an input if desired.	General Purpose Input. May be switched to an output if desired.
10	Clock	Clock Output	Clock Input
15	SCL	I^2C Master Clock Output	I^2C Slave Clock Input
16	SDA	I^2C Master Data	I^2C Slave Data
19	Cable Detect	Allows master to detect the presence of a slave device.	Ground (0VD)
2, 3, 5, 6, 8, 9, 11, 12, 17	GND	Ground (0VD)	
13, 14, 18	NC	Not Connected	

4.1.7 Fans

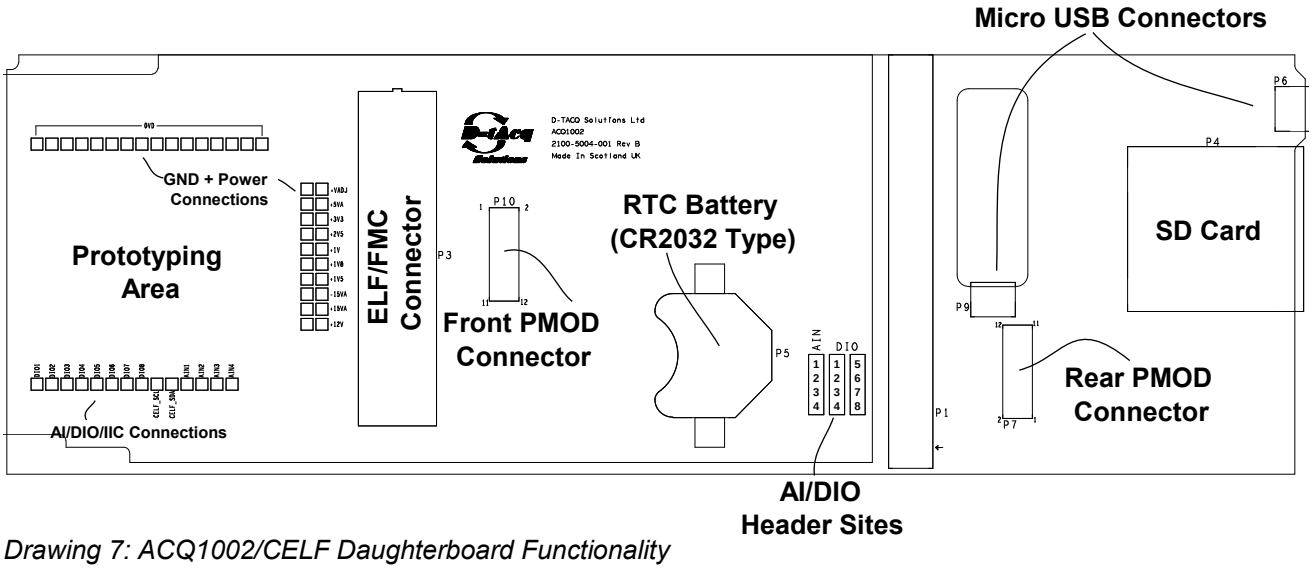
Fan outlets help keep ACQ1001 and ACQ1002 cool, drawing air across the modules from front to back. Do not cover the fan outlets.

4.1.8 Grounding Points

If required, banana plug sockets are provided for both Chassis and 0VD.

4.2 ACQ1002

ACQ1001 functionality is extended with the addition of a daughterboard (also known as a CELF). Additional features are described below.



Drawing 7: ACQ1002/CELF Daughterboard Functionality

4.2.1 PMOD

A custom rear panel may be produced along with PMOD modules allowing the user to extend the functionality of ACQ1002. For example, some customers use a GPS module to provide a synchronisation signal.

The second version of the CELF board provides a front-facing PMOD connector for further custom applications. The connector is not fitted by default to allow for the installation of full-size ELF cards, however, if required, the connector part is a Sullins NPPC062KFMS-RC.

Function	*Pin*	*Pin*	*Function*
GPIO	1	2	GPIO
GPIO (SCL[a])	3	4	GPIO
GPIO (SCL/SDA[b])	5	6	GPIO
GPIO (SDA[c])	7	8	GPIO
GND	9	10	GND
+3V3	11	12	+3V3

4.2.2 SD Card

This allows the user to add extra storage if required.

a GPIO by default, I^2C is resistor jumper selectable. Contact D-TACQ for more information.
b GPIO by default, I^2C is resistor jumper selectable. Contact D-TACQ for more information.
c GPIO by default, I^2C is resistor jumper selectable. Contact D-TACQ for more information.

4.2.3 USB

ACQ1002 contains internal and external USB 2.0 ports, allowing use of external storage or additional serial ports, for example.

The Rack and Stack cases allow for the internal mounting of standard 2.5” USB hard drives. ACQ1002R allows two modules and a hard drive. ACQ1002S allows one module and a hard drive. Please contact D-TACQ for more details on this feature.

4.2.4 Real-Time Clock

ACQ1002 also contains an internal RTC for use in timestamping remote data acquisition. The RTC takes a CR2032 type battery.

4.2.5 Digital IO

An 8-channel I²C GPIO device (Texas Instruments PCA9534[1]) is provided for slow IO use. The first two of these are used for the slot indicator LED by default, but may be disconnected by removing R21 and R22. On the second version of the CELF, all pins are connected to a header at the rear of the board, as well as the prototyping area at the front. I/O voltage is 3.3V max. Please see the device datasheet for input thresholds.

4.2.6 Analogue Inputs

A 4-channel I²C temperature and voltage monitoring device (Analog Devices AD7417[2]) is installed on the second version of the CELF to allow for slow analogue measurements. Access the inputs either at the side of the prototyping area or the header connection nearer the RTC battery holder.

WARNING!

The analogue inputs are capable of 0V to 2.5V input only. Care should be taken to ensure these limits are not exceeded. See the device datasheet for more information.

4.2.7 Prototyping Area

ACQ1002 has a standard 2.54mm/0.1” pitch prototyping area provided for custom applications. Test points are provided for multiple ground connections, every power rail, and all AI, DIO and I²C connections. See Drawing 8 for a diagram showing each connection.

Modifications are performed at the customer's own risk – D-TACQ are not responsible for failures resulting from customer modifications.

Analogue Supplies

Please contact D-TACQ for available current on each supply rail as this is customer-specific.

Two connections are provided for each supply.

Note that +VADJ is typically connected to +1V8 but this may be customer-specific so please measure to confirm voltage before use.

Analogue power rails (shown as ±VA below but marked ±15VA on the PCB) are customer-specific and may be different. Please measure to confirm voltage before use.

Multiple ground connections are provided to 0VD.

1 http://www.ti.com/product/pca9534
2 http://www.analog.com/en/analog-to-digital-converters/temperature-to-digital-converters/ad7417/products/product.html

Digital I/O

See the above section 4.2.5 for details on the eight DIO[1-8] connections. Note that DIO1 and DIO2 are also used for the front panel LED (active low). If necessary these may be disconnected by removing R21 and R22 on the underside of the board. Please also note the 3.3V input voltage limit.

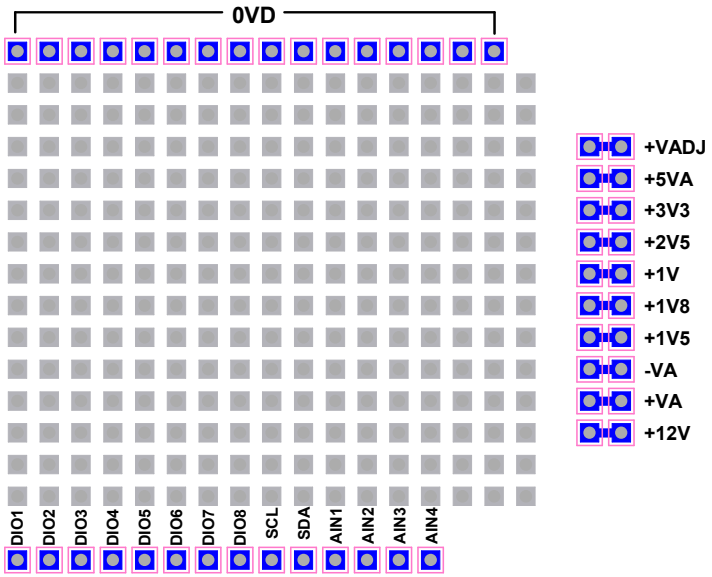
Analogue Inputs

See the above section 4.2.6 for information on the analogue inputs. Note that on some boards the power supplies may be being monitored on the AD7417 IC. To disconnect these for custom use, remove the eight resistors R61-R68 next to U12 on the top and bottom of the board. Please also note the 0-2.5V input limits.

I²C Connections

Connections to the CELF's I²C bus (running at 3.3V) are shared with some of the on-board devices. Reserved addresses are as follows:

Address	*Device*	*Function*
0x20	PCA9534	Digital I/O
0x28	AD7417	Analogue Inputs
0x6F	MCP7940N	Real-time Clock



Drawing 8: Connections on Prototyping Area

5 D-TACQ ELF/FMC Card Replacement

The modular ELF or FMC cards may be replaced by the user. Contact D-TACQ for more detailed instructions.

Warning!

Third-party cards may not be compatible with the D-TACQ mechanical superset of the FMC specification and undesired effects may occur. ACQ1001Q-ELF and ACQ1002R/S-ELF include power rails on the mezzanine connectors for D-TACQ ELF cards and therefore only use certain pins for FPGA connections.

ACQ1001 and ACQ1002 are a complex electronic assemblies. Special care should be taken in handling. The cards are susceptible to damage by ESD and improper power connections or FPGA configurations.

1. Ensure ESD precautions (chassis and body grounding) are taken before and during the opening of the case.
2. Please be extremely careful to ensure correct card alignment when plugging in the cards to avoid mezzanine card pin damage.

5.1 Case Opening

1. Remove the 6 screws which hold on the lid, then remove.
2. Remove the screws on each of the front and rear panels, then remove. Note that on Rev 1 Rack cases, the bottom-centre screw may be fixed.
3. Remove the 6 screws on the bottom which hold the two side panels.

5.2 Mezzanine Card Removal

5.2.1 Single

1. Remove the 2 screws on the underside at the front. The two on the top at the front may be left attached.
2. Remove the 2 screws on top at the rear of the module. Remove the 2 screws in the centre of D-TACQ Extended Length cards.
3. Carefully lift the card away from the mezzanine connector. Note that not a lot of force is required to do this and the card should not bend.

5.2.2 Rack

1. Follow the instructions for the Single case for both modules.

5.2.3 Stack

1. Remove the 2 screws on top at the rear of the module. Remove the 2 screws in the centre of D-TACQ Extended Length cards.
2. Carefully lift the card away from the mezzanine connector. Note that not a lot of force is required to do this and the card should not bend.
3. Remove the screws at the rear of the ACQ1002 Extension board. Remove the four standoffs in the middle of the Extension board.
4. Carefully lift the extension board away from the ACQ1001 board, taking great care to keep the backplane and connectors vertical at all times.
5. Follow the instructions for the Single case to remove the remaining module.

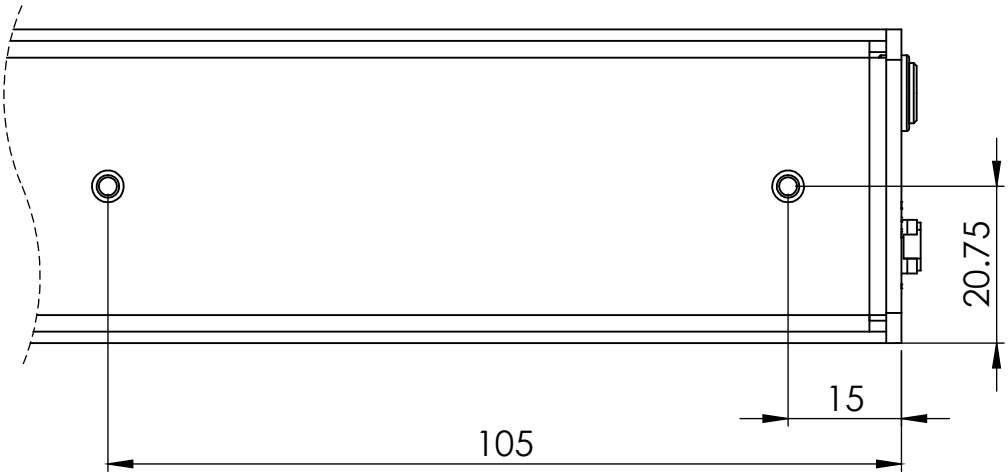
5.3 Card replacement and Case Closing

1. Follow the above instructions in reverse order.
2. Ensure the correct FPGA and Software images are installed prior to powering up.

6 Mounting Options

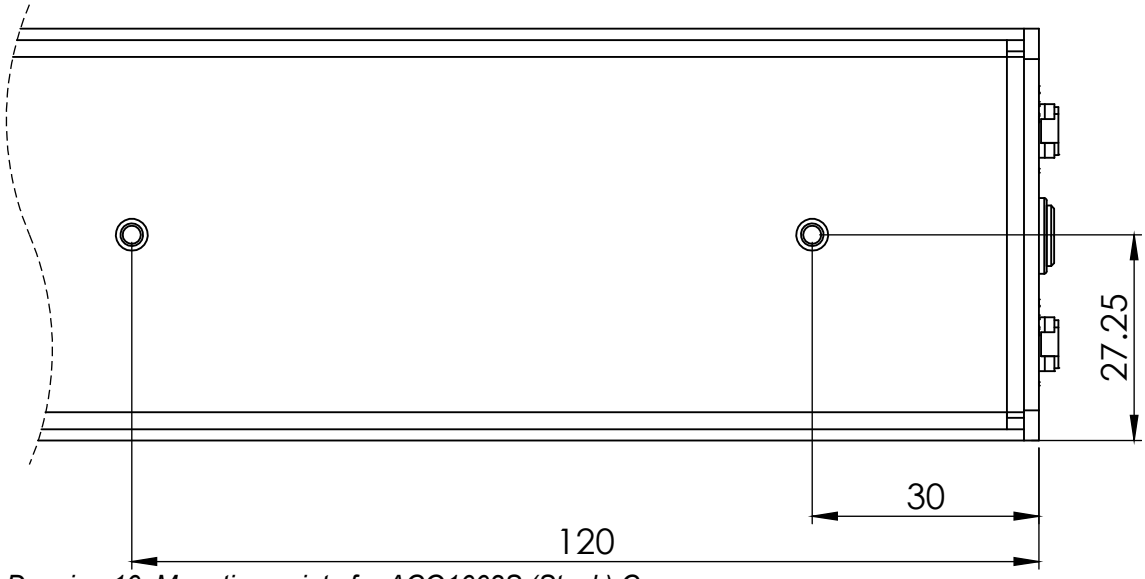
There are several different mounting options for ACQ1001 and ACQ1002. The cases can be mounted on their own via integrated fixing points – shown in the below images, referenced to the bottom and front panels. Alternatively, different options may be attached to D-TACQ's 19” mounting bracket.

6.1 Single and Rack



Drawing 9: Mounting points for ACQ1001Q (Single) and ACQ1002R (Rack) Cases

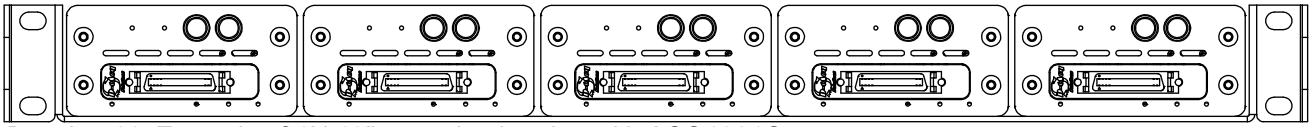
6.2 Stack



Drawing 10: Mounting points for ACQ1002S (Stack) Case

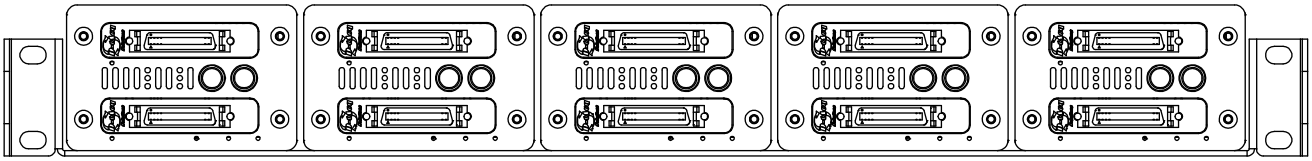
6.3 Mounting Bracket

Different examples of configurations using the ACQ1001/ACQ1002 19” Mounting Bracket are shown below. Cases may also be arranged vertically. The mounting bracket can be used for many different combinations of both ACQ1001 and ACQ1002, in both horizontal and vertical orientations. Please contact D-TACQ for your specific requirements.

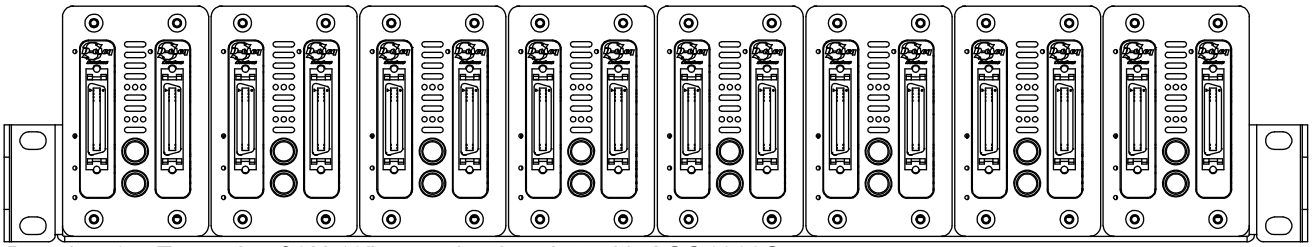


Drawing 11: Example of 1U 19" mounting bracket with ACQ1001Q

Drawing 12: Example of 1U 19" mounting bracket with ACQ1002R



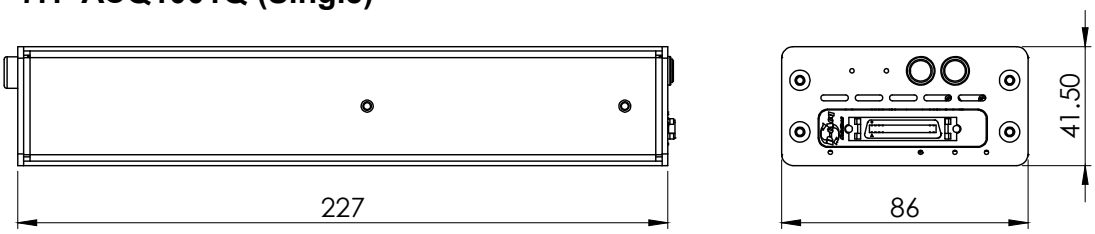
Drawing 13: Example of 19" mounting bracket with ACQ1002S



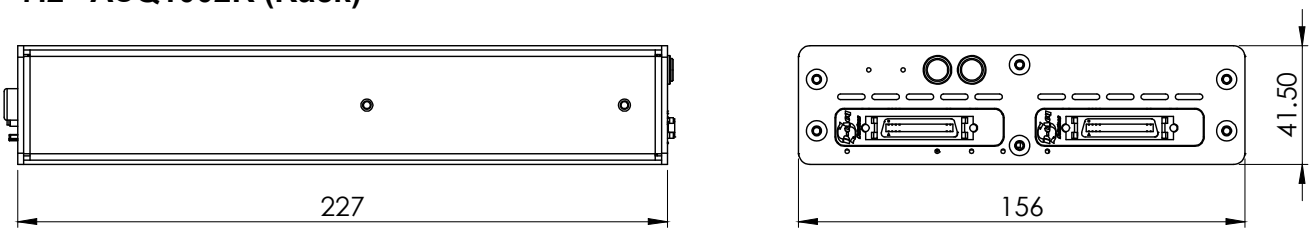
Drawing 14: Example of 2U 19" mounting bracket with ACQ1002S

7 Dimensions

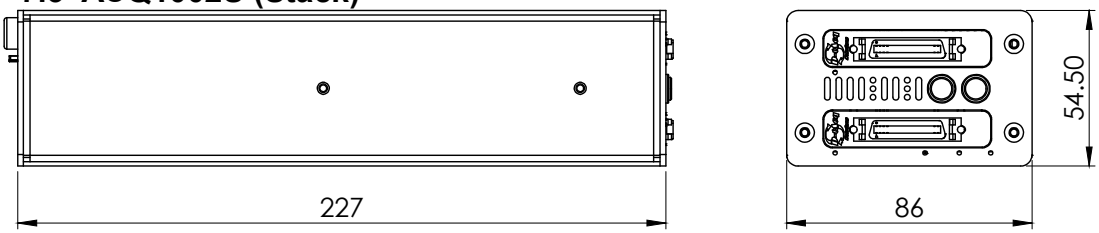
7.1 ACQ1001Q (Single)



7.2 ACQ1002R (Rack)



7.3 ACQ1002S (Stack)



8 Electrical Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*
Power					
V_{SUP}	External Supply Voltage		12		V
P	Power Consumption, dependent on payload.		15	25	W
P_{SITE}	Power per Site, dependent on payload.		10		W
Front Panel Clock					
$V_{C-IN-MAX}$	Absolute Maximum	-0.5		7	V
V_{C-IN}	Recommended Input Voltage	0		3.3 5	V
V_{C-IL}	Input Low Voltage			0.65	V
V_{C-IH}	Input High Voltage	2.65			V
Front Panel Trigger					
$V_{T-IN-MAX}$	Absolute Maximum	-0.5		6.5	V
V_{T-IN}	Recommended Input Voltage[1]	0		5	V
V_{T-IL}	Input Low Voltage			1.5	V
V_{T-IH}	Input High Voltage	3.5			V
HDMI Sync Bus					
$V_{S-IN-MAX}$	Absolute Maximum Input Voltage	-0.5		4.6	V
$I_{S-OUT-MAX}$	Absolute Maximum Continuous Output Current			±50	mA
V_{S-IN}	Recommended Input Voltage	0		3.3	V
I_{S-OL}	Recommended Low Level Output Current			12	mA
I_{S-OH}	Recommended High Level Output Current			-12	mA
V_{S-IL}	Input Low Voltage			0.8	V
V_{S-IH}	Input High Voltage	2			V
V_{S-OL}	Output Low Voltage (I_{S-OL} = 12mA)			0.7	V
V_{S-OH}	Output High Voltage (I_{S-OH} = -12mA)	2.3			V
Environmental					
	Operational	0		50	ºC
	Non-Operational	-10		85	ºC

1 This may be reduced to 3.3V as a custom solution. Please contact D-TACQ for details.

9 Changelog

Date	*Rev*	*Section*	*Changes*	*Author*
April 8, 2014	3	4.1.6	GPIO description.	Peter Johnston
		4.2	Updates for Rev B ACQ1002/CELF including diagram.	
Nov 12, 2014	4	4.2.7	More info on Prototyping area.	Peter Johnston
July 22, 2015	5	8	Electrical Specs added.	Peter Johnston