ACQ164CPCI Programmers Reference Manual

Title: **ACQ164CPCI Programmers Reference Manual**

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Revision History

Revision	Description	Date	Approval
1	Initial Discussion	11th August 2009	John McLean
2	Various updates including channel mapping table	14th September 2009	John McLean
3	SPI FLASH	23rd September 2009	John McLean
4	OverSampling Functionality	19h November 2010	John McLean
5	Introduce EXT_MAS bit for when DIO is the clock but Mastering so internal DIV8	28th August 2012	John McLean

Table of Contents

1 Introduction

This Specification describes the programming interface between the 80321 CPU and the ACQ164CPCI FPGAs.

1.1 Applicable Documents

Intel® 80321 I/O Processor,Developer's Manual 273517-002

2 Intel 80321/IOP321 Setup and Core Logic Functional Description

The Core Logic has the function of gluing the IOP321 processor to the Xilinx Spartan 3 FPGA, to the PCI bus, and all the peripheral functions in the platform. The key logic components are the 2 Core Logic CPLDs .

2.1 PBI Chip Selects

The IOP321 communicates with the peripheral logic on the PBI bus. The PBI bus is a flexible bus architecture allowing communication with devices of various widths and various speeds, the bus provides a simple mode of operation for communication with FLASH memory and it is in this mode that the bus should be used. 6 Chip selects are provided and they are utilised as follows

Each CS is used by the control logic to activate the functions listed. The 80321 supports many types of peripheral bus devices and it is important that the 80321 PBI Base Address Registers (PBBAR) are setup correctly for each of the logic functions. The following table reflects the recommended coding.

CS Function Bus Width Address To Data Wait States Recovery Cycle Wait States Flash Window Enabled

Chip Select	***Description***	Bus Width	Address To Data Wait States	Recovery Cycle Wait States	Flash Window
0	FLASH Memory	16			1 Enabled
1	Core Logic CPLDs	8			1 Enabled
2	FPGA Communications to ADC logic	32			0 Disabled
3	Serial Port UART on the RTM	8			1 Enabled
4	Ethernet Controller on the RTM	32			1 Enabled
5	Digital I/O on the RTM	32			1 Enabled

2.2 Interrupts

The IOP321 receives interrupts from multiple sources, there are 4 directly connected interrupts and a XINT1..4 and a HPI interrupt – although names HPI (High Priority Interrupt) all sources can be be used as either general purpose interrupts or as a source for the FIQ (Fast Interrupt) for the ARM core. The interrupts are connected as follows

Interrupt	*Description*
XINT0	FPGA Interrput – Used to control the core real time data movement
XINT1	RTM Ethernet interrupt
XINT2	RTM UART Interrupt.
XINT3	Not Used
HPI	System Controller Interrupt.

2.3 FLASH Memory

The FLASH Memory on the board consists of an Intel Strataflash 28F128J3.This device is a 16 MByte part and has a symmetrical block architecture consisting of 128 x 128 KByte Blocks. The device is Flash Data Integrator (FDI) and Common Flash Interface (CFI) compatible.

2.4 I^2C Devices

The IOP321 has two separate I^2C buses, the first bus is used for internal I^2C devices and the second is used for CPCI backplane devices (for the future !)

the I^2C device chain is as follows

Device Type	*B7-B3 Code*	*Typical Devices*
Temperature Monitoring	5	Temperature Monitoring is provided by 2 x Analog Devices AD7417 devices. These are dual function devices containing a temperature sensor and 4 x analog inputs which are multiplexed onto the ADC to provide a 4 channel ADC function The 2 devices are connected as follows. Device 000 Channel 0 Temperature Output. Device 001 Channel 0 Temperature Output. In the I^2C Scan on the IOP321 these devices appear at 28_h and 29_h
Clock Generation	D	Clock Generation is provided by a Real Time Clock. Device 000 – Dallas DS1338 Real Time Clock. This device provides real time clock functionality and 56 bytes of battery backed NVRAM. Dallas DS1338 is hard coded at 00 In the I^2C Scan on the IOP321 this device appears at 68_h
Memory SPD	A	The Core Logic supports 1 x 200 pin DDRSDRAM DIMM socket which has been set up for a single DIMM SPD device at Device 0 In the I^2C Scan on the IOP321 this device appears at 50_h
Memory SPD Protection	6	As Per above In the I^2C Scan on the IOP321 this device appears at 30_h
RTM DAC Reference Potentiometer	5	This devices is used to trim the 10V reference to set up the +10V reference signals. The device used is an Analog Devices AD5280 Device 101 +10V Trim Potentiometer

Device Type	*B7-B3 Code*	*Typical Devices*
		In the I^2C Scan on the IOP321 this device appears at $2d_h$

2.5 Core Logic CPLDs

There are 2 Core CPLDs in the ACQ164CPCI design, they are similar but not identical to the 2 Core Logic CPLDs in the 2G platform.

1 – The System Controller

2 – The Digital I/O Controller

These two CPLDs are described in the following sections. The IOP321 communicates with the Core CPLDs using the PBI bus see Section 3 for details

2.5.1 The System Controller CPLD

The System Controller provides the following functions

Board Reset Controller

PCI Bus Arbitration when in System Controller mode

IOP321 External Interrupt Controller

2.5.1.1 Reset Controller

The board reset controller senses whether the board is in a System Slot or a Peripheral Slot and responds to the incoming Reset as follows

System Slot

The whole board is reset if either the following reset sources are active

Rear Panel Push Button / Power Up Reset

CPCI Push Button Reset

JTAG Reset

The board operates as a 33 MHz 32/64 bit system controller.

Peripheral Slot

The board is reset when the PCI reset is active

When in a Peripheral Slot the PCI Clock Drivers are disabled and the arbiter is disabled.

2.5.1.2 PCI Bus Arbiter

The PCI Bus Arbiter implements a fair arbitration scheme between the masters on the Compact PCI backplane. devices this may be enhanced in the future to provide 2 levels of priority but at present it is simply a rotating arbitration scheme.

2.5.1.3 IOP321 External Interrupt Controller

The external Interrupt Controller provides System Controller interrupt handling for the IOP321,

NOTE The UART Interrupt is on XINT2 not in the External Interrupt Controller which differs from the 2G Platform

These interrupt sources are as follows

Bit	*Name*	*Description*
0	S_INTAn	Secondary Bus PCI Interrupt A – Soft System Slot Mode only
1	S_INTBn	Secondary Bus PCI Interrupt B – Soft System Slot Mode only
2	S_INTCn	Secondary Bus PCI Interrupt C – Soft System Slot Mode only
3	S_INTDn	Secondary Bus PCI Interrupt D – Soft System Slot Mode only

The Interrupt controller is a simple level triggered interrupt with each interrupt source having a simple mask bit. The Control and Status Registers are described later.

The Interrupt Controller produced a wire OR'd output of the selected interrupts and signals the interrupt on the IOP321 HPIn pin.

2.6 The Digital I/O Controller

The Digital I/O Controller provides the following functions

FPGA Loading

High Speed Digital I/O cross-point switching

IOP321 PBI Bus Data Buffer Control

2.6.1 FPGA Loading

FPGA Loading is performed by writing byte wide information into the SelectMAP port of the FPGA. The sequence is as follows

Set the PROGRAM pin to 0

Set the PROGRAM pin to 1

Write the data into the FPGA

Check the state of the DONE pin

If correct then the FPGA has been successfully loaded.

2.6.2 High Speed Digital I/O Crosspoint Switch

Operation of the high speed Digital I/Os differs from the 1st Generation in that this CPLD acts as an active switch rather than the bunch of analog switches previously used. This results in improved signal integrity at the expense of a small time delay allowing the clock lines to be run at higher frequencies. In addition to this some lines are defined as wired Or'd signals allowing Trigger lines to be activated from various sources.

Digital I/Os 0-2 are defined as Clocks and as such the input signals are connected to the outputs

Digital I/Os 3-5 are defined as Trigger/Event signals and in this case the input signals are merely ANDed with the output enables for a Wired OR'd Open drain arrangement

Full details of the programming of these switches is found in xxxx

3 Core CPLD System Interface

3.1 Memory Maps

3.1.1 CPLD Memory Map.

19_h	FPGA Data Register
18_h	FPGA Control Register
15_h	Digital I/O Bit 5 Control Register
14_h	Digital I/O Bit 4 Control Register
13_h	Digital I/O Bit 3 Control Register
12_h	Digital I/O Bit 2 Control Register
11_h	Digital I/O Bit 1 Control Register
10_h	Digital I/O Bit 0 Control Register
	Revision Register
	Reset Control / Satus Register
01_h	Interrupt Status Register
00_h	Interrupt Control Register

3.2 Core CPLD Register Definitions

This section defines the programming model for the Control and Status in the Core CPLDs.

All the Control /Status Registers are 8 bits wide, they must be accessed with byte wide commands since the PBI bus is decoding the width code explicitly for each bus cycle.

Each register definition includes a table with 4 lines. Line 1 shows the bits defined by the table. Line 2 defines the name of the register or the name of the bit fields in the register. Line 3 defines the operations possible on the register bits as follows.

RO This bit is a read-only bit
WO This bit is a write-only bit
R/W This bit is a readable and writeable
R/C This bit can be cleared by writing a 1 to its location. This bit can also be read without affecting its condition.

Line 4 defines the state of the bit following a reset operation as defined below.

P This bit is affected by a power-on reset
S This bit is affected by a Primary Bus Reset
X This bit is not affected by any reset

3.2.1 00_h Interrupt Control Register

This 5 bit read/write only register is used to control the enabling of the external PCI Interrupts when the board is in System Controller Mode.

BIT	4	3	2	1	0
NAME	HPI/XINT3	INTDn	INTCn	INTBn	INTAn
OPER	WO	WO	WO	WO	WO
RESET	0 PS	0 PS	0 PS	0 PS	0 PS

INTAn This bit controls the enabling of the PCI bus Interrupt line A
0 = Interrupt Disabled
1 = Interrupt Enabled

INTBn This bit controls the enabling of the PCI bus Interrupt line B
0 = Interrupt Disabled
1 = Interrupt Enabled

INTCn This bit controls the enabling of the PCI bus Interrupt line C
0 = Interrupt Disabled
1 = Interrupt Enabled

INTDn This bit controls the enabling of the PCI bus Interrupt line D
0 = Interrupt Disabled
1 = Interrupt Enabled

HPI/XINT3 This bit allows the PCI interrupts to be redirected to XINT3 from the standard HPI Interrupt.
0 = Use HPI Interrupt
1 = Use XINT3 Interrupts
NOTE : This bit is only available on Rev 5 or Higher Versions of the CPLD.

3.2.2 01_h Interrupt Status Register

This 5 bit read only register is used to check the status of the external PCI Interrupts when the board is in System Controller Mode.

BIT	5	3	2	1	0

NAME	INTn	INTDn	INTCn	INTBn	INTAn
OPER	RO	RO	RO	RO	RO
RESET	0 PS	0 PS	0 PS	0 PS	0 PS

INTAn This bit hows the status of the PCI bus Interrupt line A
1 = Interrupt Inactive
0 = Interrupt Active

INTBn This bit hows the status of the PCI bus Interrupt line B
1 = Interrupt Inactive
0 = Interrupt Active

INTCn This bit hows the statusof the PCI bus Interrupt line C
1 = Interrupt Inactive
0 = Interrupt Active

INTDn This bit shows the status of the PCI bus Interrupt line D
1 = Interrupt Inactive
0 = Interrupt Active

INTn This but shows the status of the output interrupt
1 = Interrupt Inactive
0 = Interrupt Active

3.2.3 02_h Reset Control / Status Register

This 54 bit read/write only register is used to generate a Soft Reset on the board and to determine the current PCI Configuration of the board. The Soft Reset Function generates a hardware reset on the board under software control.

BIT	3	2-1	0
NAME	Reserved	PCI_ENV	SOFTRESET
OPER	RO	RO	WO
RESET	0 PS	X PS	0 PS

SOFTRESET This bit controls the enabling of the Soft Reset function.
0 = Soft Reset Inactive
1 = Soft Reset Active

PCI_ENV These bits are used to determine the PCI Environment of the board according to the following table.
00 System Slot Master – The board is plugged into the System Slot and PCI is enabled
01 Peripheral Mode - The board is plugged into a Peripheral Slot and PCI is enabled
10 Stand Alone Mode - The board is isolated from the PCI Bus
11 Illegal State.

3.2.4 03_h Revision Register

This 4 bit read only register indicates the current revision of the System Controller CPLD it should be used to detect System Slot Controller Functionality.

BIT	3-0
NAME	REVISION
OPER	RO
RESET	X PS

REVISION These bits indicate the current revision of the CPLD.
Current Revision = 2
System Slot Controller Functionality is available for Revision 2 and Above

3.2.5 10_h – 15_h Digital I/O Control Registers Bits 0 to 5

These 6 bit write only registers are used to control the Fast Digital I/O resource Input Analog to Digital data acquisition process. Each bit of Digital I/O has a 6 bit control register associated with it with the following definition

BIT	7-6	5-4	3	2	1	0
NAME	Reserved	INP_SEL	PXI_EN	RP_EN	MEZZ_EN	FPGA_EN
OPER	WO	WO	WO	WO	WO	WO
RESET	0 PS	00 PS	0 PS	0 PS	0 PS	0 PS

INP_SEL These bits control which input bus will be used as the input source for this bit
00 = FPGA
01 = Mezzanine
10 = Rear Panel
11 = PXI

PXI_EN This bit controls whether the output will be activated for this bit on the PXI Bus
0 = Output Tri-Stated
1 = Output Active

RP_EN This bit controls whether the output will be activated for this bit on the Rear Transition Module
0 = Output Tri-Stated
1 = Output Active

MEZZ_EN This bit controls whether the output will be activated for this bit on the Mezzanine Module
0 = Output Tri-Stated
1 = Output Active

FPGA_EN This bit controls whether the output will be activated for this bit to the Control FPGA
0 = Output Tri-Stated
1 = Output Active

It should be noted that it is not possible to have a bit that is both an input and an output, the input select logic will override any output selection, i.e. if the IN_SEL is set to Rear Panel then the RP_EN bit will be ignored and the signal will be used as an input.

3.2.6 18_h FPGA Control / Status Register

This 8 bit read / write register is used to control FPGA programming and to determine the status of the loading on the FPGA

BIT	7	6-3	2	1	0
NAME	PROGRAM	Reserved	FPGA_INIT	FPGA_BUSY	FPGA_DONE
OPER	WO	RO	RO	RO	RO
RESET	0 PS	0 PS	X PS	X PS	X PS

FPGA_DONE This bit reflects the status of the DONE pin on the FPGA
0 = DONE pin low (Load in progress)
1 = DONE pin high (Load in complete)

FPGA_BUSY This bit reflects the status of the BUSY pin on the FPGA.
0 = FPGA not busy
1 = FPGA busy loading data byte
A 1 should never be seen on this bit.

FPGA_INIT This bit reflects the status of the INIT pin on the FPGA
0 = Goes low while PROGRAM is active and stays low until memory is cleared
1 = Init Complete and FPGA Ready to Load

PROGRAM This bit controls the PROGRAM Pin on the FPGA
0 = PROGRAM pin active (0)
1 = PROGRAM pin Inactive (1)

To Load the FPGA the PROGRAM pin must be set to 0 for at least 10 uS and then be set high. Programming should not commence until the INIT pin has been sampled high.

3.2.7 19_h FPGA Data Register

This 8 bit register is used as the write location for the FPGA data, data should be written as a sequential bytes, no special timing is required, bytes may be written as quickly as desired

4 RTM Control CPLD

The RTM Control CPLD provides the following functions

Decode of the SMSC LAN91C111 Ethernet MAC+PHY Controller

Decode of the Digital I/O Logic

4.1 SMSC LAN91C111 Ethernet MAC+PHY Controller

The LAN91C111 Ethernet Controller is decoded on its own CS line as described in Section 2.1. The interface is set by the PBI as 32 bits wide, the LAN91C111 device recognises the 80321 byte lane enable lines which allows byte, word, or dword data widths to be accessed.

The chip is accessed on it's asynchronous port, the fasted possible PBI bus cycle in Flash Mode ties closely with the recommended fastedst access modes on the LAN91C111 therefore making the asynchronous mode the most effective bus interface connection

The DATACSn data port on the LAN91C111 is decoded by the RTM Control CPLD to provide the possibility of direct access and/or DMA access to the data port on the device. The decode of the data port is at two places 0x380 when used for PIO access and 0x400-0x7ff when used for DMA. It is important that the default 0x300 address of the LAN91C111 is not changed since it could cause overlap with the DATACSn decode .

4.2 Digital I/O Decode

The Digital I/O decode is set at 32 bits wide although the registers are only 16 bit wide. This is to ensure compatibility with the rest of the 2G boards some of which may only have a 16 bit PBI bus on the RTM.

The RTM provides 32 bits of individually programmable Digital I/Os. These are powered with medium performance 24mA symmetrical drive TTL devices providing a flexible digital I/O subsystem for low to medium frequency digital I/Os

5 RTM Control CPLD System Interface

5.1 Digital I/O Control / Status Registers Memory Map

Address	*Description*
10_h	Digital I/O Bank B Data Register
$0C_h$	Digital I/O Bank A Data Register
08_h	Digital I/O Bank B Direction Register
04_h	Digital I/O Bank A Direction Register
00_h	Digital I/O Control Register

5.2 Register Definitions

This section defines the programming model for the Control and Status registers in the functional control FPGA.

All the Control /Status Registers are 32 bits wide, they must be accessed with long word commands

Each register definition includes a table with 4 lines. Line 1 shows the bits defined by the table. Line 2 defines the name of the register or the name of the bit fields in the register. Line 3 defines the operations possible on the register bits as follows.

RO This bit is a read-only bit
WO This bit is a write-only bit
R/W This bit is a readable and writeable
R/C This bit can be cleared by writing a 1 to its location. This bit can also be read without affecting its condition.

Line 4 defines the state of the bit following a reset operation as defined below.

P This bit is affected by a power-on reset
S This bit is affected by a Primary Bus Reset
X This bit is not affected by any reset

5.2.1 00_h Digital I/O Control Register

This 32 bit read / write register is used for overall control of the Digital I/Osr

BIT	*31-8*	*7-4*	*3-2*	*1*	*0*
NAME	Not Used	REVISION	Not Used	DIREN	REGCLRn
Operation	R/O	R/O	R/W	R/W	R/W
Reset	fffff PSR	1	00 PSR	0 PSR	0 PSR

REGCLRn Register Clear
This clears the outputs latches for the outputs on Bank A and Bank B
0 = Registers Cleared = Set to 0
1 = Registers Available for writing

DIREN Direction Registers Enable
This bit enables the outputs on the Direction Control Registers
0 = Direction Registers outputs disabled
1 = Direction Registers outputs enabled

Note: The two bits above ensure that when the board is powered up the 32 Digital I/Os are initially set to inputs and that the output registers are set to 0. The correct seqence for control is as follows.

1) Lift the Register Clear bit above
2) Write the desired data pattern to the Data Register bits that are to be outputs
3) Write the I/O pattern to the Direction Registers
4) Enable the DIREN bit to activate the outputs.

Once the initial pattern is setup changes can be made at any time to the Direction or Data registers to change the I/O assignments

The 32 bits of digital I/O are output in two banks known as Bank A and Bank B. Bank A contains bits 0-15 and Bank B 16-31.

REVISION Revision Code of the CPLDr
This code can be used to detect functions/bug fixes in the CPLD.
The current Revision Levels are in the wild.
F = Pre Revision code capable CPLD – working Etehrnet and RS232 inoperational Digital I/O
1 = Fully working CPLD.

5.2.2 04_h Digital I/O Bank A Direction Register

This 32 bit read / write register is used to control the direction of the 16 bits of Digital I/Os in Bank A

BIT	*31-16*	*15- 0*
NAME	Not Used	DIREN*x*n
Operation	R/O	R/W
Reset	fffff PSR	0 PSR

DIREN*x*n Direction Control for bit x
This bit defines the direction of each Digital I/O in bank A
0 = Bit is an Output
1 = Bit is an Input

5.2.3 08_h Digital I/O Bank B Direction Register

This 32 bit read / write register is used to control the direction of the 16 bits of Digital I/Os in Bank B

BIT	*31-16*	*15- 0*
NAME	Not Used	DIREN*x*n
Operation	R/O	R/W
Reset	fffff PSR	0 PSR

DIREN*x*n Direction Control for bit x
This bit defines the direction of each Digital I/O in bank B
0 = Bit is an Output
1 = Bit is an Input

5.2.4 $0C_h$ Digital I/O Bank A Data Register

This 32 bit read / write register is used to control the output data of the 16 bits of Digital I/Os in Bank A

BIT	*31-16*	*15- 0*
NAME	Not Used	DATA*x*
Operation	R/O	R/W
Reset	fffff PSR	0 PSR

DATA*x* Data bit for bit x
This bit defines the data to be output on the appropriate bit on Digital I/O in bank A
0 = Bit is at TTL 0
1 = Bit is at TTL 1

5.2.5 10_h Digital I/O Bank B Data Register

This 32 bit read / write register is used to control the output data of the 16 bits of Digital I/Os in Bank B

BIT	*31-16*	*15- 0*
NAME	Not Used	DATA*x*
Operation	R/O	R/W
Reset	fffff PSR	0 PSR

DATA*x* Data bit for bit x
This bit defines the data to be output on the appropriate bit on Digital I/O in bank B
0 = Bit is at TTL 0
1 = Bit is at TTL 1

6 ACQ164CPCI FPGA Functional Description

The ACQ164CPCI System FPGA communicates with the Intel 80321 processor on its' Peripheral Bus Interface (PBI). It controls the ADC devices and receives the ADC data and transmits it to the 80321 as a sequence of burst transfers. The ADC132CPCI System FPGA receives data from 8 ADC FPGAs, each ADC FPGA receives data from 4 ADC devices to from the 32 channel system.

6.1 System PBI Interface Characteristics

The FPGA utilises the 80321 PBI interface in the following way

32 bit wide 100MHz PBI in standard mode. 1 Chip Select dedicated to the FPGA

Support for non-burst transfers to the Registers. Access to the ADC data FIFO is by burst access only. Burst only access uses pipelined reads with 1 wait state performance.

3 decode areas in the FPGA

1 for Control Status Registers

1 for the ADC FIFO this address is also used as a write address for the direct mapped DAC data when DACs are fitted to the RTM

1 for the DAC Waveform Memory when DACs are fitted to the RTM

The Overall Address map is as follows. This is the offset from the base address set by the PBI Base Address Register 2 (PBBAR2)

Note: The PBI Limit Register 2 (PBLR2) must be set to at least 4 Mbytes i.e. 0x00400000

Address	*Description*
Offset 00200000_h	HAWG Waveform Memory for DACs 1 & 2
Offset 00100000_h	ADC FIFO and FAWG DAC Memory
Offset 00000000_h	Control and Status Registers

The DAC Memory is split as follows

HAWG (Hardware Arbitary Waveform Generator). This memory is used when high speed updates are required, it consists of a 512 sample waveform memory specifically for DAC channels 1 and 2. This memory is used in conjunction with the Waveform Limit Register to fully define the length of waveform required. The HAWG memory is only used when the HAWG has been activated in the DAC Control Register.

FAWG (FIFO assisted software Arbitrary Waveform Generator) DAC Memory is a FIFO that is used when a software driven arbitrary waveform is being used, this allows medium speed updates with the flexibility of larger memory depth provided by the main processor memory. The FIFO consists of a 32 sample memory with FIFO Pointer indication provided by the FIFO Status Register

Interrupt capability on programmable events

6.2 Data FIFO Arrangement

The Host is decoupled from the data Acquisition process by using FIFO memory.

The FIFO organisation is as follows

Each ADC subsystem has a separate buffer FIFO where the data is read simultaneously from the two banks of ADCs.. These FIFOs are known as “COLD” FIFOs
These FIFOs are 513x32 in size (2Kbytes) providing buffer storage for up to 16 samples

A PBI buffer FIFO known as the HOT FIFO is used to gather the information from the 2 ADC FIFOs to

provide a single access point for the 80321
This FIFO is 8Kx32 in size (32 Kbytes) providing buffer storage for 128 samples

6.2.1 ADC FPGA Channel Allocation

The diagram below shows the channel connection to the ADC FPGAs

6.2.2 FIFO Data Ordering

Due to layout constraints on the board the ADC data is mangled as it arrives on the board the software must remap the channels according to the following table

Connector Pinout	*Column*	*Row*	*Readout Order*	*DAC*
1	1	1	1	1
2	1	2	5	2
3	1	3	9	3
4	1	4	13	4
5	2	1	2	5
6	2	2	6	6
7	2	3	10	7
8	2	4	14	8
9	3	1	3	9
10	3	2	7	10
11	3	3	11	11
12	3	4	15	12
13	4	1	4	13
14	4	2	8	14
15	4	3	12	15
16	4	4	16	16
17	4	5	20	17
18	4	6	24	18
19	4	7	28	19
20	4	8	32	20
21	3	5	19	21
22	3	6	23	22
23	3	7	27	23
24	3	8	31	24
25	2	5	18	25
26	2	6	22	26
27	2	7	26	27
28	2	8	30	28
29	1	5	17	29
30	1	6	21	30
31	1	7	25	31
32	1	8	29	32

7 FPGA System Interface

7.1 FPGA Control / Status Registers Memory Map

7.1.1 System FPGA

Address	*Description*
C0h	LLC Register Copy Area
80_h	Interrupt Control Register
58_h	SPI FLASH Control/Data Register
54_h	Clock Speed Estimator Register
$4C_h$	Transient Length Register
48_h	Time Counter Latched Register
44_h	Time Counter Immediate Register
$2C_h$	Waveform Address Limit Register
28_h	ADC Offset Adjust DACs Control Register
24_h	Digital I/O Control / Status Register
20_h	Clock Data Register – Not used at present
$1C_h$	Clock Control Register
18_h	DAC Control Register
14_h	ICS527 Control Register
10_h	OverSampling Register
$0C_h$	ADC Control Register
08_h	FIFO Status Register
04_h	FIFO Control Register
00_h	Board Debug Register

7.2 Register Definitions

This section defines the programming model for the Control and Status registers in the functional control FPGA.

All the Control /Status Registers are 32 bits wide, they must be accessed with long word commands

Each register definition includes a table with 4 lines. Line 1 shows the bits defined by the table. Line 2 defines the name of the register or the name of the bit fields in the register. Line 3 defines the operations possible on the register bits as follows.

RO This bit is a read-only bit
WO This bit is a write-only bit
R/W This bit is a readable and writeable
R/C This bit can be cleared by writing a 1 to its location. This bit can also be read without affecting its condition.

Line 4 defines the state of the bit following a reset operation as defined below.

P This bit is affected by a power-on reset
S This bit is affected by a Primary Bus Reset
X This bit is not affected by any reset

7.2.1 00_h Board Debug / Revision Register Register

This 32 bit read / write register is used for revision control and as a 32 bit test register

BIT	***31-0***
NAME	PATTERN
Operation	R/W
Reset	“DEADBEEF” PSR

For compatibility reasons this register shall read “DEADBEEF when register read. After the first write to the register a read shall return the FPGA revision code, subsequent writes shall return the value written.

Current revision code support is as follows

0x00000300 Initial revision
0x00000301 Include SPI FLASH Register
0x00000302 For Trigger and Event Debug Complete
0x00000305 OverSampling Functionality
0x00000306 EXT_MAS Functionality

The register can be reset to it's initial state by writing the Rev_Reg_Reset bit in the Control Register.

7.2.2 04_h FIFO Control Register

This 32 bit read/write register is used to control the data acquisition FIFOs.

BIT7	*31*	*30*	*29*	*28*	*27-24*
NAME	DAC_IE	Not Used	DAC_RESET	DAC_ENABLE	DAC_LTIDE
Operation	R/W	R/W	R/W	R/W	R/W
Reset	0 PSR	0 PSR	1 PSR	0 PSR	0000 PSR

DAC_IE Tide Mark Interrupt Enable
This bit enables the Tide Mark Interrupt
0 = Interrupt Disabled
1 = Interrupt Enabled

DAC_RESETFIFO Reset
This bit controls the reset of the FIFO, setting the read and write pointers to 0
0 = No Effect
1 = Reset the read and write pointers of the FIFO

DAC_ENABLE FIFO Enable
This bit enables the FIFO allowing the Acquisition Process to read from the DAC FIFO
0 = Read from the FIFO is disabled
1 = Read from to the FIFO is enabled

DAC_LTIDE Low Tide Mark Threshold
Sets the FIFO Level at which the Low Tide Mark Interrupt will be made

BIT	*23-17*	*16*	*15-14*	*13*	*12*
NAME	Not Used	THROW_EN	Not Used	Not Used	Not Used
Operation	R/W	R/W	R/W	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	0 PSR	0 PSR

BIT	*11*	*10*	*9*	*8*
NAME	ADC2_RESET	ADC2_ENABLE	ADC1_RESET	ADC1_ENABLE
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	0 PSR

THROW_EN Enable sample Throw Away Logic
0 = No Throw Away Logic FIFO Overflow as normal
1 = Throw Away Samples when FIFOs are in danger of overflowing

ADCX_RESET FIFO Reset
This bit controls the reset of the FIFO, setting the read and write pointers to 0
0 = No Effect
1 = Reset the read and write pointers of the FIFO

ADCX_ENABLE FIFO Enable
This bit enables the FIFO allowing the Acquisition Process to write to the ADC FIFO
0 = Write to the FIFO is disabled
1 = Write to the FIFO is enabled

BIT	*7*	*6*	*5*	*4-0*
NAME	HOT_IE	HOT_RESET	HOT_ENABLE	HOT_HTIDE
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	1 PSR	0 PSR	00000 PSR

HOT_IE Tide Mark Interrupt Enable
This bit enables the Tide Mark Interrupt
0 = Interrupt Disabled
1 = Interrupt Enabled

HOT_RESET FIFO Reset
This bit controls the reset of the FIFO, setting the read and write pointers to 0
0 = No Effect
1 = Reset the read and write pointers of the FIFO

HOT_ENABLE FIFO Enable
This bit enables the FIFO allowing the Acquisition Process to write to the ADC FIFO and the HOT FIFO
0 = Write to the FIFO is disabled
1 = Write to the FIFO is enabled

HOT_HTIDE High Tide Mark Threshold
Sets the FIFO Level at which the High Tide Mark Interrupt will be made in the HOT FIFO
A Tide mark of 0 will generate an interrupt as soon as there is any data in the HOT FIFO, this value should be used when in Low Latency Mode.

At least one ADC FIFO must be enabled when the HOT FIFO is enabled. It is recommended that all FIFO enables be set /cleared at the same time.
Individual enables can be used to activate only those ADC banks required for 32/64 channels of operation.

7.2.3 08_h FIFO Status Register

This 32 bit read/clear register is used to control the data acquisition FIFOs.

BIT7	***31***	***30***	***29-24***
NAME	DAC_TR	FAWG_OVER	FAWG_POINTER
Operation	R/O	R/O	RO
Reset	0 PSR	0 PSR	00000 PSR

DAC_TR DAC Triggered Flag
0 = DAC Subsystem has not Triggered
1 = DAC Subsystem has Triggered
Writing a 1 to this bit clears the flag

FAWG_OVER FAG FIFO Overflow
0 = FAWG FIFO OK
1 = FAWG FIFO Overflow
Writing a 1 to this bit clears the flag

FAWG_POINTER FAWG FIFO Pointer Position
These bits define the status of the FAWG FIFO and indicates how much data is currently in the FIFO
Each bit in the pointer is equivalent to one samples worth of data in the FIFO i.e. 32 bytes

BIT	***23***	***22***	***21***	***20***
NAME	ADC_EV1	ADC_EV0	ADC_TR	LL_TIME_TRIG
Operation	R/C	R/C	RO	RO
Reset	0 PSR	0 PSR	0 PSR	0 PSR

BIT	***19***	***18***	***17***	***16***
NAME	THROW	Reserved	Reserved	Reserved
Operation	R/C	RO	RO	RO
Reset	0 PSR	0 PSR	0 PSR	0 PSR

BIT	***15***	***14***	***13***	***12***
NAME	Reserved	ADC2_NE	ADC2_OVER	ADC2_UNDER
Operation	RO	RO	R/C	R/C
Reset	0 PSR	0 PSR	0 PSR	0 PSR

BIT	***11***	***10***	***9***	***8***
NAME	Reserved	ADC1_NE	ADC1_OVER	ADC1_UNDER
Operation	RO	RO	R/C	R/C
Reset	0 PSR	0 PSR	0 PSR	0 PSR

ADC_EV1 Event 1 Detected Flag
0 = No Event Detected
1 = Event Detected
Writing a 1 to this bit clears the flag

ADC_EV0 Event 0 Detected Flag
0 = No Event Detected
1 = Event Detected
Writing a 1 to this bit clears the flag

ADC_TR ADC System Triggered Flag
0 = ADC System is not Triggered (no Samples are being taken)
1 = ADC System is Triggered (Samples are being taken)
Writing a 1 to this bit clears the flag

LL_TIME_TRIG Low Latency Time Counter Triggered
0 = Trigger has not Occurred
1 = Trigger has Occurred
This bit should be used in conjunction with the LATENCY_TIMER setting in the ADC Control Register. When this bit is set it means that the LATENCY Timer has reached the level specified by LATENCY_TIMER setting allowing fine control from the sample clock until this bit is set and hence the ability to pipeline the start of the ADC FIFO read.

THROW Cold FIFO Data "Throw Away" Event Flag
0 = No data Thrown Away
1 = Data Has been Thrown Away
Writing a 1 to this bit clears the flag

ADCX_NE ADC FIFO Not Empty Flag
0 = ADC FIFO Empty
1 = ADC FIFO Not Empty

ADCX_OVER ADC FIFO Overflow Flag
0 = ADC FIFO is not in overflow
1 = ADC FIFO has overflowed i.e. A write was made to a Full FIFO
Writing a 1 to this bit clears the flag
This bit should never be set since the ADC state machines are designed to drop out if the ADC FIFO ever becomes Full

ADCX_UNDER ADCX FIFO Underflow Flag
0 = ADCX FIFO is not in underflow
1 = ADCX FIFO has underflowed i.e. A read was made to an Empty Full FIFO
Writing a 1 to this bit clears the flag
This bit should never be set unless the HOT to COLD copy system is in error..

The COLD FIFO in the ACQ196CPCI is not a fixed FIFO, it can be any of the 2 ADC FIFOs depending on what has been enabled. In general it is set to be the last FIFO to be read in the COLD-HOT copy operation i.e in 64 channel mode it is the FIFO for ADC Bank 2, in 32 channel mode it is ADC bank 1

BIT	***7***	***6***	***5***	***4***	***3-0***
NAME	HOT_HT	HOT_OVER	HOT_UNDER	HOT_NE	HOT_POINTER
Operation	RO	R/C	R/C	RO	RO
Reset	0 PSR	0 PSR	0 PSR	0 PSR	0000 PSR

HOT_HT High Tide Mark Level Reached
This bit indicates that the Tide Mark Level has been reached
0 = FIFO is below the Tide Mark Level
1 = FIFO is above the Tide Mark Level

HOT_OVER HOT FIFO Overflow Flag
0 = HOT FIFO is not in overflow

1 = HOT FIFO has overflowed i.e. A write was made to a Full FIFO
Writing a 1 to this bit clears the flag
This bit will be set if the 80321 does not respond to a High Tide state with a read of the Acquisition data in the FIFO

HOT_UNDER HOT FIFO Underflow Flag
0 = HOT FIFO is not in underflow
1 = HOT FIFO has under flowed i.e. A read was made to an Empty Full FIFO
Writing a 1 to this bit clears the flag
This bit should never be set unless the system reads too much data from the FIFO.

HOT_NE HOT FIFO Not Empty Flag
0 = HOT FIFO is Empty
1 = HOT FIFO contains data

HOT_POINTER HOT FIFO Pointer Position
These bits define the status of the HOT FIFO and indicates how much data is currently in the FIFO.

7.2.4 $0C_h$ ADC System Control Register

This 32 bit read/write register is used to control the Acquisition Process for the ADCs

BIT	***31***	***30-27***	***26-24***
NAME	Rev_Reg_Reset	Not Used	OTR_MASK
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	000 PSR

REV_REG_RESET This bit when set resets the Debug/ Revision register to it's initial state. The reset requires a write of the value 1 followed by a write of the value 0.

OTR_MASK Output Trigger Select Bits
The Trigger Source is synchronised to the DIV8 sample clock. These bits control which Digital I/O the Synchronised Trigger output on.
00 = No Digital I/O selected – External Trigger Disabled
01 = Digital I/O 3
10 = Digital I/O 4
11 = Digital I/O 5

BIT	***21***	***20***	***19***	***18-16***
NAME	CODING	LL_MODE	TR_EDGE	TR_MASK
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	000 PSR

CODING ADC Data Coding
This bit defines whether the ADC data is coded as 2's complement or straight binary. The straight binary mode is used when the board is configured for unipolar operation.
0 = 2's Complement
1 = Offset Binary

LL_MODE Low Latency Mode
This bit defines whether the ADC state machine will convert in Low Latency or High Throughput Mode
0 = High Throughput Mode
1 = Low Latency Mode

TR_EDGE Trigger Edge Sense Definition
This bit determines the edge that will be detected by the Trigger Detector
0 = Falling Edge
1 = Rising Edge

TR_MASK Trigger Digital I/O Selector Definition
These bits determine digital I/O that will be used as the source for the Trigger Detector
000 = No Digital I/O selected – External Trigger Disabled
001 = Digital I/O 0
010 = Digital I/O 1
011 = Digital I/O 2
100 = Digital I/O 3
101 = Digital I/O 4
110 = Digital I/O 5
Others = Reserved for Future Functions.

BIT	***15***	***14-12***	***11***	***10-8***
NAME	EVENT1 EDGE	EVENT1 DIO	EVENT0 EDGE	EVENT0 DIO
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	000 PSR	0 PSR	000 PSR

The EVENT Detector is controlled by two fields; the EVENT EDGE bit and the EVENT DIO vector. These bits define the event that will be used to generate an embedded event and cause the EVENT_FLAG bit in the FIFO Control Register to be set. The fields are described as follows

EVENTX_EDGE Event Definition Edge Sense
This bit determines the edge that will be detected by the Event Detector
0 = Falling Edge
1 = Rising Edge

EVENTX_DIO Event Definition Digital I/O Selector
These bits determine digital I/O that will be used as the source for the Event Detector
000 = No Digital I/O selected – Edge Detector Disabled
001 = Digital I/O 0
010 = Digital I/O 1
011 = Digital I/O 2
100 = Digital I/O 3
101 = Digital I/O 4
110 = Digital I/O 5
Others = Reserved for Future Functions.

BIT	***7***	***6***	***5-4***
NAME	LLSYNC	CLKDIV	ADC_MODE
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR

LLSYNC This bit activates the Low Latency Clock Synchronisation feature. This re-loads the clock divider when a trigger arrives to provide a fixed phase relationship between the divided clock and the trigger
0 = Normal Divider Operation
1 = Low Latency Clock Synchronisation Active

CLKDIV

ADC_MODE ADC Operational Mode
These bits define which mode of operation the ADS1278 chips are used in, they form the following combinations.

CLKDIV	ADC_MODE	Output Rate
1	00 = High-Speed	/256
1	01 = High-Resolution	/512
0	10 = Low-Power	/256
1	10 = Low-Power	/512
0	11 = Low-Speed	/512
1	11 = Low-Speed	/2560 -- not supported

BIT	***3***	***2***	***1***	***0***
NAME	EC_STA	TRIGGERED	SOFTTRG	ACQEN
Operation	RO	RO	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	0 PSR

EC_STA External Clock Status.
This bit indicates the current logic level of the Clock
0 = External Clock at logic 0
1 = External Clock at logic 1

TRIGGERED System Triggered
This status bit indicates that the Acquisition system has been triggered.
0 = Not Trigger Received

1 = Trigger Received

SOFTTRG Soft Trigger
This bit control can be used to generate a Software Trigger for the board. This has identical functionality to a Hardware Trigger. The Software must generate a falling edge for a trigger to occur i.e. This bit must be set high then set low.

ACQEN Acquisition Enable
This bit controls the Acquisition process
0 = Acquisition Disabled
1 = Acquisition Enabled

7.2.5 10_h ADC OverSampling Register

This 32 bit read/write register is used to control the OverSampling on the ADCs

BIT	***31-8***	***7-0***
NAME	Not Used	ACCUM_VAL
Operation	R/W	R/W
Reset	0 PSR	000 PSR

ACCUM_VAL Accumulation values

These bits set the number of sample that are to be accumulated before being stored..

0 = Store Every Sample

1 = Accumulate 2 and Store

2 = Accumulate 3 and Store

255 = Accumulate 256 and Store

7.2.6 14_h ICS527 Control Register

This 32 bit read/write is used to control the PLL device that is used to generate the output frequency of the Internal Clock. The external PLL device is an ICS-527-1 - check the manufacturer's data sheet for additional information

BIT	***31-24***	***22-16***
NAME	Not Used	FDW
Operation	W/O	W/O
Reset	"00000" PSR	"00000000" PSR

BIT	***14-8***	***7-6***	***5-0***
NAME	RDW	S1 S0	Not Used
Operation	W/O	R/W	R/W
Reset	"0000000" PSR	"00" PSR	"000" PSR

FDW Feedback Divider Word (FDW) = 0 to 127

RDW Reference Divider Word (RDW) = 0 to 127

S1 S0 Output Frequency Range Table
00 = 37 → 75 MHz
01 = 18 → 37 MHz
10 = 4 → 10 MHz
11 = 75 → 160 MHz

The Output Frequency from the On Board Clock Generator when using the Local Oscillator is as follows

$$\text{Output Frequency} = 32.768\ \text{MHz} \times \frac{FDW+2}{RDW+2}$$

The value for RDW must also meet the following criteria

$$300\ \text{kHz} < \frac{\text{Input Frequency}}{RDW+2}$$

7.2.7 18_h DAC System Control Register

This is not implemented at present

This 32 bit read/write register is used to control the Acquisition Process for the DACs

BIT	***31-24***	***24***	***23***	***22***
NAME	Not Used	DAC_2CH	WAVE_REG	Not Used
Operation	R/O	R/C	R/W	R/W
Reset	000 PSR	0 PSR	0 PSR	0 PSR

BIT	***21***	***20***	***19***	***18-16***
NAME	CODING	LL_MODE	TR_EDGE	TR_MASK
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	000 PSR

DAC_2CH DAC 2 Channel mode

This bit indicates that the FAWG is operating in 2 channel mode to reduce bus occupancy.
0 = 16 channel mode
1 = 2 channel mode

WAV_REG Waveform / Register Mode
This bit defines whether the DAC data for channels 1 & 2 will be sourced from the DAC data registers or from the Waveform memory
0 = Register Mode
1 = Waveform Mode

CODING DAC Data Coding
This bit defines whether the ADC data is coded as 2's complement or straight binary. The straight binary mode is used when the board is configured for unipolar operation.
0 = 2's Complement
1 = Straight Binary

LL_MODE Low Latency Mode
This bit defines whether the DAC state machine will convert in Low Latency Clocked Mode, in Low latency mode the DAC value is updated as soon as it is loaded and in Clocked Mode it is output on the next clock.
0 = High Throughput Mode
1 = Low Latency Mode

TR_EDGE Trigger Edge Sense Definition
This bit determines the edge that will be detected by the Trigger Detector
0 = Falling Edge
1 = Rising Edge

TR_MASK Trigger Digital I/O Selector Definition
These bits determine digital I/O that will be used as the source for the Trigger Detector
000 = No Digital I/O selected – Trigger Disabled
001 = Digital I/O 0
010 = Digital I/O 1
011 = Digital I/O 2
100 = Digital I/O 3
101 = Digital I/O 4
110 = Digital I/O 5
Others = Reserved for Future Functions.

BIT	***15***	***14-12***	***11***	***10-8***
NAME	Not Used	Not Used	Not Used	Not Used
Operation	R/W	R/W	R/W	R/W
Reset	0 PSR	000 PSR	0 PSR	000 PSR

BIT	***7***	***6-5***	***4***
NAME	EC_RISING	EC_MASK	EXTCLK
Operation	R/W	R/W	R/W
Reset	0 PSR	000 PSR	0 PSR

EC_RISING External Clock Polarity
This bit controls the polarity of the selected External Clock
0 = External Clock is Falling Edge
1 = External Clock is Rising Edge

EC_MASK External Clock Select
These bits are used to select which Digital I/O line will be used as the External Clock Source for the data acquisition process.
00 = External Digital I/O 0

01 = External Digital I/O 1
10 = External Digital I/O 2
11 = Soft Clock

EXTCLK External Clock
This bit controls whether the Clock will be sourced from the Internal Clock Generator or from and External Source
0 = Internal Clock Generator
1 = External Source set by the EC_MASK bits

BIT	*3*	*2*	*1*	*0*
NAME	CLKVAL	TRIGGERED	SOFTTRG	ACQEN
Operation	RO	RO	R/W	R/W
Reset	0 PSR	0 PSR	0 PSR	0 PSR

EC_STA External Clock Status.
This bit indicates the current logic level of the selected External Clock
0 = External Clock at logic 0
1 = External Clock at logic 1

TRIGGERED System Triggered
This status bit indicates that the Acquisition system has been triggered.
0 = Not Trigger Received
1 = Trigger Received

SOFTTRG Soft Trigger
This bit control can be used to generate a Software Trigger for the board. This has identical functionality to a Hardware Trigger. The Software must generate a falling edge for a trigger to occur i.e. This bit must be set high then set low.

ACQEN Acquisition Enable
This bit controls the Acquisition process
0 = Acquisition Disabled
1 = Acquisition Enabled

7.2.8 $1C_h$ ADC Clock Control Register

This 32 bit read/write register is used to control the the Internal Clock Generator, and the capability of driving a clock signal out on a Digital I/O line.

BIT	*31*	*30*	*29-16*
NAME	SCLK_RESET	SCLK_LOCK	
Operation	R/W	R/W	
Reset	0 PSR	X PSR	00

SCLK_RESET Reset the SCLK DCM A Reset is achieved by toggling the signal high and then returning it to 0

SCLK_LOCK Lock Status of the SCLK DCM
0 = DCM has lost LOCK a RESET is required
1 = DCM is Running

BIT	*15*	*14*	*13-12*
NAME	OIND_POL	Not Used	OIND_MASK
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	00 PSR

BIT	***11***	***10***	***9-8***
NAME	IND_POL	Not Used	IND_MASK
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	00 PSR

BIT	***7***	***6***	***5-4***
NAME	OCS_POL	Not Used	OCS_MASK
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	000 PSR

BIT	***3***	***2***	***1-0***
NAME	CS_POL	EXT_MAS	CS_MASK
Operation	R/W	R/W	R/W
Reset	0 PSR	0 PSR	00 PSR

OIND_POL Index Pulse Mask Output Polarity
0 = Falling Edge
1 = Rising Edge

OIND_MASK Index Pulse Mask Output
These bits control if and which Digital I/O the Index marking of the phase of the ICS Clock divide by 8 will be output on.
00 = No Digital I/O
01 = External Digital I/O 0
10 = External Digital I/O 1
11 = External Digital I/O 2

IND_POL Input Index Pulse Polarity
0 = Falling Edge
1 = Rising Edge

IND_MASK Index Pulse Mask Input
These bits control if and which Digital I/O the Clock Index marking the phase of the Input Clock will be used
00 = No Digital I/O
01 = External Digital I/O 0
10 = External Digital I/O 1
11 = External Digital I/O 2
Note: if IND_MASK is set to 00 the device generates an internal index pulse

OCS_POL Clock Source Polarity
0 = Falling Edge
1 = Rising Edge

OCS_MASK Clock Output Mode Select
These bits control if and which Digital I/O the ICS Clock will be output on. Note this is not the full speed ICS clock – it is a divide by 8 known as the DIV8 signal in order to avoid high speed clock transitions on the backplane.
00 = No Digital I/O
01 = External Digital I/O 0
10 = External Digital I/O 1
11 = External Digital I/O 2

CS_POL Clock Source Polarity
0 = Falling Edge
1 = Rising Edge

EXT_MAS External Clock Master
This bit defines the external clock source when in Master Mode. This causes the logic to still utilise the

internally generated DIV8 allowing the board to utilise an independent External Clock.
0 = Use CS_MASK for both ICS clock and for DIV8
1 = Use CS_MASK for ICS only use internal DIV8

CS_MASK Clock Source Mask.
These bits define which source will be used as the input clock for the ICS synthesiser used to generate the modulator and shift clock.
00 = 32.768 MHz on-board Local Oscillator
01 = External Digital I/O 0
10 = External Digital I/O 1
11 = External Digital I/O 2

Note:
There are three main modes of operation that can be configured from the Clock and Index selections, those as standard in concept to the PCI modes. They are:-

Stand-Alone – The board neither generates or accepts External Clock or Index pulses and uses self generated versions of these signals for internal use in timing. This is the default/reset condition
Example Configuration
CS_MASK = 00 -- SCLK Generated from Local Oscillator
OCS_MASK = 00 -- Do not Output The Clock
IND_MASK = 00 -- Use Internal Index generation.
OIND_MASK = 00 -- Do not Output The Index Pulse

Master Mode – The board generates External Clock and Index Pulses. The board generates the ICS timing independently and does not use External Clock as the ICS Clock Source. The board uses the External Index pulse for the purposes of generating the synchronisation signals to ensure multi-board synchronisation.
Example Configuration
CS_MASK = 00 -- SCLK Generated from Local Oscillator
OCS_MASK = 10 -- Generate Clock on DIO 1
IND_MASK = 11 -- Receive Index on DIO 2
OIND_MASK = 11 -- Generate Index on DIO 2

Slave Mode - The board accepts both External Clock and Index Pulses. The board uses the External Clock as a fixed x 8 multiplier for the ICS Clock. The board uses the External Index and Clock pulses for the purposes of generating the synchronisation signals
Example Configuration
CS_MASK = 10 -- SCLK Generated from DIO 1
OCS_MASK = 00 -- Do not Output The Clock
IND_MASK = 11 -- Receive Index on DIO 2
OIND_MASK = 00 -- Do not Output The Index Pulse

7.2.9 24_h Digital I/O Control / Status Register

This 32 bit read/write register is used to direct the digital I/Os for use in Clocking and Triggering the acquisition process.

BIT	***31-24***	***23-16***	***15-8***	***7-0***
NAME	Not Used	SETOUT	OUTDAT	INPDAT
Operation	R/O	R/W	R/W	R/O
Reset	“00” PSR	“0000” PSR	“0000” PSR	“XXXX” PSR

SETOUT Digital I/O Direction
These bits set the direction for the DIOs – bit 23 is mapped to DIO7, 22 to DIO6 etc.

0 = DIOx is an Input
1 = DIOx is an Output

OUTDAT Digital Output Data.
These bits contain the digital output data that will be set when the corresponding bit of the direction is set. Bit 15 is mapped to bit 7 of the DIOs – bit 14 is mapped to DIO6 etc.
0 = DIOx output is at logic 0
1 = DIOx output is at logic 1

INPDAT Digital Input Data.
These bits contain the DIOs input data. If the DIO is set as an output this will duplicate the data bit in the Digital Output Data (if there is a difference it can be used to diagnose shorted outputs etc), if it is set as an input it will reflect the data on the external signal.
0 = DIOx input is at logic 0
1 = DIOx input is at logic 1

7.2.10 28_h ADC Offset Adjust DACs

This 32 bit read/write register is used to control the DACs for Offset Trim. The Offset Trim DACS consist of 8 octal DAC devices. In each write one channel on each DAC is updated,

DAC 1A	ADC 13 Offset Adjust	DAC 1B	ADC 14 Offset Adjust
DAC 1C	ADC 15 Offset Adjust	DAC 1D	ADC 16 Offset Adjust
DAC 1E	ADC 17 Offset Adjust	DAC 1F	ADC 18 Offset Adjust
DAC 1G	ADC 19 Offset Adjust	DAC 1H	ADC 20 Offset Adjust
DAC 2A	ADC 9 Offset Adjust	DAC 2B	ADC 10 Offset Adjust
DAC 2C	ADC 11 Offset Adjust	DAC 2D	ADC 12 Offset Adjust
DAC 2E	ADC 21 Offset Adjust	DAC 2F	ADC 22 Offset Adjust
DAC 2G	ADC 23 Offset Adjust	DAC 2H	ADC 24 Offset Adjust
DAC 3A	ADC 5 Offset Adjust	DAC 3B	ADC 6 Offset Adjust
DAC 3C	ADC 7 Offset Adjust	DAC 3D	ADC 8 Offset Adjust
DAC 3E	ADC 25 Offset Adjust	DAC 3F	ADC 26 Offset Adjust
DAC 3G	ADC 27 Offset Adjust	DAC 3H	ADC 28 Offset Adjust
DAC 4A	ADC 1 Offset Adjust	DAC 4B	ADC 2 Offset Adjust
DAC 4C	ADC 3 Offset Adjust	DAC 4D	ADC 4 Offset Adjust
DAC 4E	ADC 29 Offset Adjust	DAC 4F	ADC 30 Offset Adjust
DAC 4G	ADC 31 Offset Adjust	DAC 4H	ADC 32 Offset Adjust

BIT	***31***	***30***	***29-26***	***25-16***
NAME	CHIPSEL	HSHAKE	DACX_ADDR	DACX_DATA
Operation	R/W	R/0	R/W	R/W
Reset	0 PSR	0 PSR	0000 PSR	X000 PSR

CHIPSEL Start the DAC Write Process
This bit controls whether the DAC Data is transmitted to the Offset Trim DACs
0 = No DAC Update
1 = Start DAC Update

HSHAKE DAC Update Hand Shake.
This bit indicates the state of the load process into the Offset Trim DACs
0 = Load Complete
1 = Load In Progress

DACX_ADDR DAC X Address
These bits contain the address of the channel on DAC X to be updated
0000 = No DACs updated
0001 = DAC 0 is to be updated
0010 = DAC 1 is to be updated
0011 = DAC 2 is to be updated
0100 = DAC 3 is to be updated
0101 = DAC 4 is to be updated
0110 = DAC 5 is to be updated
0111 = DAC 6 is to be updated
1000 = DAC 7 is to be updated
1111 = All DACs updated

DAC1_DATA DAC 1 Data
These bits contain the 10 bit data for the selected channel in DAC 1

BIT	*15-14*	*13-10*	*9-0*
NAME	Not Used	DACY_ADDR	DACY_DATA
Operation	R/W	R/W	R/W
Reset	00 PSR	0000 PSR	0000 PSR

DACY_ADDR DAC Y Address
These bits contain the address of the channel on DAC Y to be updated
See DACY_ADDR for the bit definitions

DACY_DATA DAC Y Data
These bits contain the 8 bit data for the selected channel in DAC Y

The DAC update process is as follows
A single write to the register sends an update pattern to 2 DACs, the DACs are loaded as a serial chain. By performing 2 writes, every DAC in the chain is written to, the values are then updated on all the devices by setting the CHIPSEL high.
The DAC chain is as follows 8 → 7 → 6 → 5 → 4 → 3 → 2 → 1
The data is shifted out of the Offset adjust Register from the left therefore DACX_DATA is sent before DACY_DATA.

7.2.11 $2C_h$ WaveForm Limit Register

This 24 bit read/write register is used to control the memory operation for the HAWG and SAWG

BIT	*31-24*	*23-16*	*8-0*
NAME	Reservered	FAWG_DIV	WAVLIMIT
Operation	R/O		R/W
Reset	0 PSR		111111111 PSR

FAWG_DIV Clock divider that divides down the rate from the Sample Clock at which the SAWG FIFO is accessed to allow low overhead waveform production

WAVLIMIT Upper address in the DAC waveform memory at which the waveform counter will wrap back to 0 at

7.2.12 44_h Time Counter Immediate Register

This 32 bit read only register contains current value of the Time Counter

BIT	*31*	*30-26*	*25-24*	*23-12*	*11-0*
NAME	RUNNING	Not Used	*TCS_MASK*	Not Used	TIME_COUNTERI
Operation	R/O	R/W	RW	R/O	R/O
Reset	X PSR	000PSR	00 PSR	fffPSR	000PSR

RUNNING This bit indicates whether the Time Counter is running
0 = Time Counter Not Running
1 = Time Counter Running

TCS_MASK Time Counter Clock Source.
These bits define which source will be used as the clock for the Time Counter.
000 = External Digital I/O 0
001 = External Digital I/O 1
010 = External Digital I/O 2
011 = External Digital I/O 3

100 = External Digital I/O 4
101 = External Digital I/O 5
Others = Internal Clock

The TIME_COUNTERI data is a direct reading of the current value of the value of the counter, this is debounced during the read to avoid roll-over effects

7.2.13 48_h Time Counter Latched Register

This 32 bit read only register contains current value of the Time Counter the Analog Inputs were clocked.

BIT	***30-12***	***11-0***
NAME	Not Used	TIME_COUNTERL
Operation	R/O	R/O
Reset	000PSR	000PSR

The TIME_COUNTERL data is the latched value of the counter

7.2.14 48_h Repeat Gated / Transient Triggered Control

This 32 bit read / write register controls the Repeated Gate Mode / Repeated Transient Length Modes of Opperation.

BIT	***31-30***	***29-16***	***15-0***
NAME	MODE	Not Used	TRANSLENGTH
Operation	R/W	R/O	R/W
Reset	00PSR	0000PSR	0000PSR

MODE These bits define a Gated Mode of Operation a Transient Mode of Operation and a Combined Mode as follows

00 Normal Operation
01 Transient Operation
Acquisition Starts after a Trigger and continues until TRANSLENGTH samples have been acquired. Subsequent "Triggers" cause repeated captures
10 Gated Operation
Acquisition starts after a Trigger and while the Gate signal is on (DIO that the Trigger is set to) . Gate is High if the Trigger is set to Rising Edge and Low is Trigger is set to a Falling Edge. Subsequent "Triggers" cause repeated captures.
11 Combined Mode
Acquisition Starts after a Trigger and continues until either a TRANSLENGTH number of samples have been acquired or until the Gate switched off. The Gate signal going off auto reloads the TRANSLENGTH register so subsequent Gate pulses will cause subsequent acquisitions following the same process as the first acquisition.

TRANSLENGTH These bits define the length of a Transient Capture

7.2.15 54_h Clock Estimator

This 32 bit register contains the result of a time/frequency estimator for a selectable Clock Source, This can be used to detect both the input frequency and output frequency of the ICS527 to ensure correct operation

BIT	*31*	*30-28*	*27-20*	*19-0*
NAME	USE_DIO	DIO_SRC	Not Used	CLK_ESTIMATE
Operation	R/W	R/W	R/W	R/O
Reset	0 PSR	000 PSR	000 PSR	"XXX" PSR

USE_DIO This bit determines whether the counter will be driven from the ICS 527 clock generator or from a DIO
0 = Clock Source is the ICS 527
1 = Clock Source is an External Digital selected by DIO_SRC

DIO_SRC DIO Clock Source Mask.
These bits define which DIO source will be used as the input clock Clock Estimator when USE_DIO is set to 1
000 = External Digital I/O 0
001 = External Digital I/O 1
010 = External Digital I/O 2
011 = External Digital I/O 3
100 = External Digital I/O 4
101 = External Digital I/O 5
110 = External Digital I/O 6
111 = External Digital I/O 7

The CLK_ESTIMATE counter is free running it counts at a fixed frequency of selected clock divided by 16 and allows the frequency to be estimated as follows.

$$Frequency = \frac{(Count_B - Count_A) * 16}{(Time_B - Time_A)}$$

It is the responsibility of the software to provide a deterministic interval to determine $Time_B$ and $Time_A$

7.2.16 58_h SPI FLASH Control / Data Register

This 32 bit register contains the control and data interface to the Atmel AT45DB321D 4 Mbyte SPI FLASH device.

The current implementation utilises the IOP SPI interface and this register only controls the Reset and Write Protect.

BIT	*31*	*30*	*29-0*
NAME	SPI_RESET	SPI_WP	Not Used
Operation	R/W	R/W	R/O
Reset	0 PSR	000 PSR	"0000" PSR

SPI_RESET This bit resets the SPI FLASH device. A reset is performed by writing a 1 to this bit and then clearing it back to 0. The RESET should remain at 1 for at least 10uS before clearing it back to 0

SPI_WP This bit puts the SPI FLASH device into a Write Protect Mode. In this mode the Sector Protection logic is applied – see device data sheet.
0 = Write Enabled
1 = Write Protected

7.2.17 80_h Interrupt Control Register

This write only register is used to enable and disable the Interrupt process from the FIFO Control/Status Register in order to facilitate an optimum data transfer process.

BIT	*31-8*	*7*	*6-0*
NAME	Not Used	HOT_INTEN	Not Used
Operation	W/O	W/O	W/O
Reset			

HOT_INTEN Interrupt Enable.
This bit masks the Tide Mark Interrupts in the FIFO Control Register to form the 80321 Interrupt.
0 = Interrupt Disabled
1 = Interrupt Enabled

7.2.18 $C0_h$ Register Copy Area

This is not implemented at present

This is a scratch pad area covering the address range $C0_h$ to FF_h for use in Low Latency applications for communication with the host.

This is not implemented at present